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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/737,124	12/17/2003	Young-Doug Kim	8947-000074/US	5936

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EXAMINER	
DANG, KHANH	

ART UNIT	PAPER NUMBER
2111	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/737,124	KIM ET AL.	
	Examiner	Art Unit	
	Khanh Dang	2111	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on 23 May 2007.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-39 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-39 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Application Status

Applicants' RCE filed 5/23/2007 to continue prosecution of this Application is acknowledged.

Interview Acknowledgement

The Examiner agrees with the content of the Interview presented by Applicants. The Examiner also continues to agree with Applicants that the pseudo-grant signals in Kenny do not begin at the same time, as claimed in amended claim 1, for example.

However, upon further review the claims and Kenny, it is the Examiner's position that the current claims, as amended, have still not been in condition for allowance. A new ground of Rejection (based on the same Kenny reference) is set forth below. The Kenny 102 Rejection is now replaced by Kenny 103 Rejection.

Any inconvenience this may cause is regretted.

Claim Rejections - 35 USC § 103

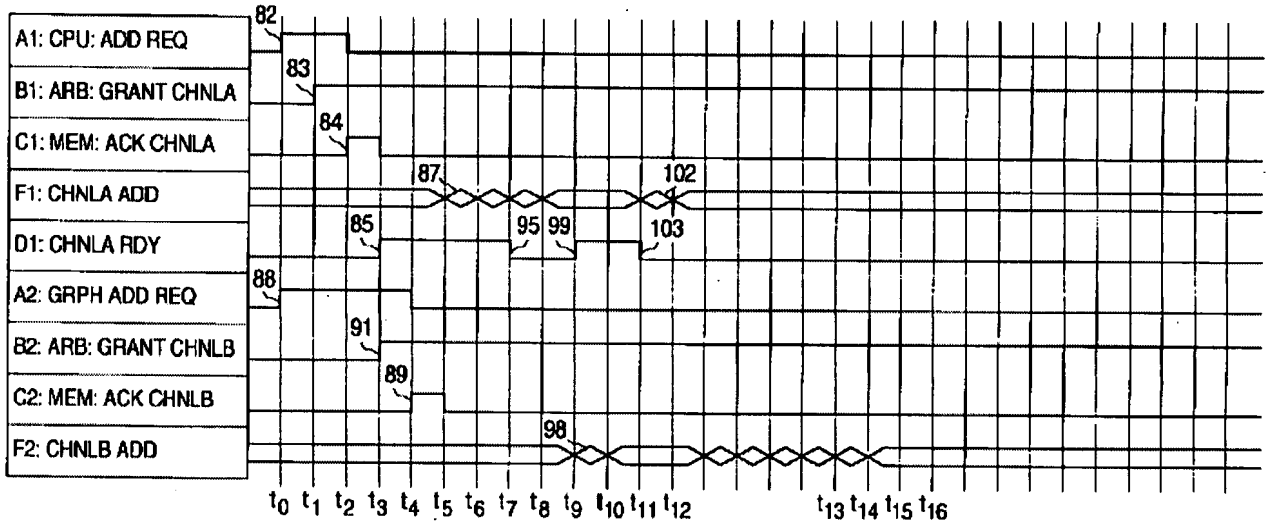
The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-10, 13-39 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kenny.

With regard to claim 1, Kenny discloses an arbiter (arbiter 4, Fig. 1, for example) in a system (shown generally at Fig. 1) for generating a pseudo-grant signal to all requesting master units (the arbiter 4 in Kenny "assigns a virtual channel to each master/slave pair requesting the data bus for data transfer between the master module and a slave module. Each virtual channel represents a timeslice on the bus and is owned by a separate master/slave pair, thereby permitting multiple master/slave pairs to have concurrent ownership of the singular data bus" (emphasis added). In another word, the arbiter 4 grants or bus ownership bus grant to the virtual channel of every requesting master before actual arbitration, wherein "data transfer between the master/slave pair commences immediately upon the arbiter asserting the appropriate 'channel active' signal." It is clear that assigning concurrent ownership (bus ownership or bus grant) of a single data bus to each master by the arbiter before actual arbitration is interpreted as providing a pseudo bus grant signal by the arbiter to each master. In particular, in Kenny, a master module initializes bus access by asserting address and bus request signals on the bus 11. The arbiter 4 and the slave module detect the address and request signals asserted by the master module. The arbiter 4 then identifies the master module making the request, determines the master module's priority, and grants a virtual channel. The virtual channel granted can be arbitrarily selected by an allocation procedure. Specifically, Kenny discloses that "concurrent ownership of the data bus by multiple master/slave pairs advantageously enhances bus

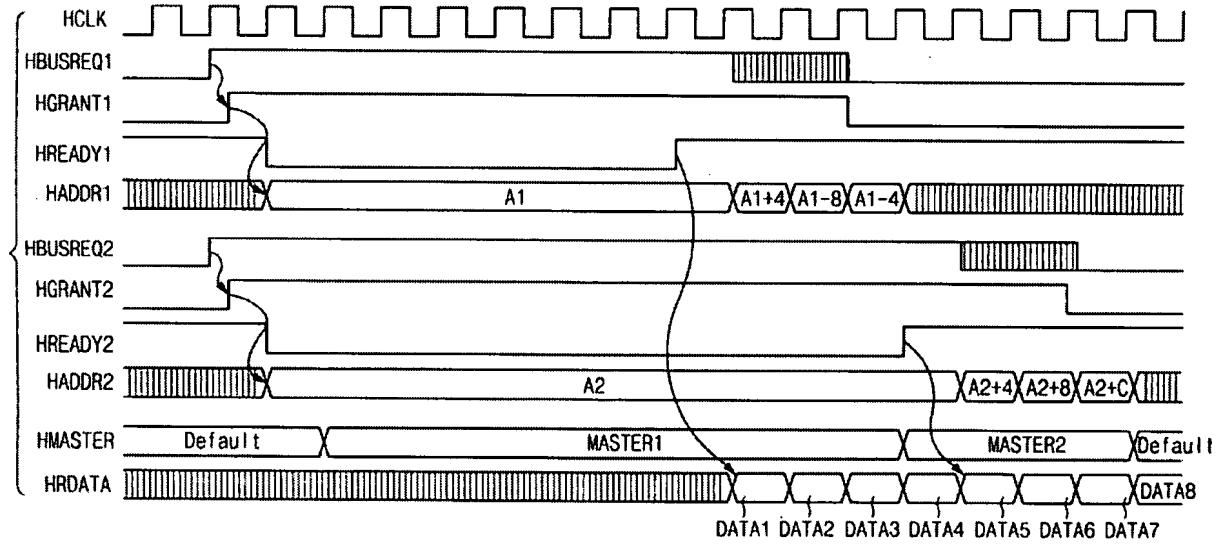
accessibility over conventional split-transaction bus protocols since the transactional overhead associated with bus re-acquisition protocols between a master/slave pair is eliminated. Since each channel, hence each master/slave pair, has its own unique channel active signal, data transfer between the master/slave pair commences immediately upon the arbiter asserting the appropriate "channel active" signal." Kenny further discloses that "FIG. 9 is a timing diagram summarizing concurrent transactions of three virtual channels of the present invention." In addition, Kenny discloses that "[a]ll concurrent virtual channel owners wait for an access grant by arbiter 4 to data bus 2. Access to data bus 3 to a particular virtual channel occurs when arbiter 4 asserts the virtual channel's active signal (e.g., CHNLA ACTIVE). Note that in Fig. 9, because the priority of each requesting master (CPU, PCI Controller, Graphics Controller) is not pre-assigned, the arbiter 4 must resolve the priority between requesting masters, and grants virtual channels A, B, C to each requesting master based on priority of each requesting master, by asserting signal GNT CHLNA, signal GNTCHLNB, and signal GNTCHLNC, at times t1, t3, and t5. Fig. 9 is reproduced below:



Kenny also discloses that the arbiter receives transaction information from all requesting master units in response to the pseudo-grant signals (after asserting signal GNT CHNLA, arbiter 4 returns to its initial state 47 to wait for the next ADD/REQ signal from each of the requesting master).

Although Kenny clearly disclose that pseudo-grant signals are generated to all the requesting masters. Kenny, as discussed above regarding Fig. 9, does not particularly disclose that the pseudo-grant signals begin at the same time, as claimed in at least Applicants' claim 1, and shown in Fig. 6, which is reproduced below:

Fig. 6



Note that in Fig. 6 above, the pseudo-grant signals HGRANT1 and HGRANT2 begin at the same time.

However, in addition to the timing for psedo-grant signals as shown in Fig. 9 above, Kenny also disclose that "[a]lternatively, each subsystem may be configured with a fixed virtual channel with a pre-assigned priority. Pre-designating virtual channels and priorities for each module simplifies processing by eliminating allocation procedures and requiring arbiter 4 to merely match the I/O address of the requesting master module to that master module's pre-assigned virtual channel and pre-assigned priority, referencing a table stored in a register of arbiter 4 or elsewhere." Thus, it is clear that by using pre-designating virtual channels and priorities for each module, the arbiter 4 does not have to arbitrate between requesting masters having different priority, and assign a virtual channel to a requesting master according to its priority.

Thus, it would have been obvious to one of ordinary skill in the art at the time the invention was made to generate pseudo-grant signals GNT CHLNA, GNTCHLNB, and GNTCHLNC to all requesting masters beginning at the same time, because by using a fixed virtual channel with a pre-assigned priority for each of the requesting master, the arbiter 4 does not have to arbitrate between masters resulting in generating/providing pseudo-grant signals to all requesting masters at different starting time. Since pseudo-grant signals GNT CHLNA, GNTCHLNB, and GNTCHLNC to all requesting masters begin at the same time, it is clear that arbitration latency can be further reduced, and as a result, the overall performance of the entire system of Kenny is improved.

With regard to claim 2, it is clear that the arbiter 4 further performs arbitration based on the transaction information such as the pre-assigned priority received from the requesting master.

With regard to claim 3, it is clear that in Kenny, the arbiter 4 includes a master interface for interfacing with the masters (see at least Fig. 1 and description thereof) for generating the pseudo-grant signal (virtual channel grant signal GNT CHNLA) to all the requesting masters, for receiving the transaction information from all the requesting master units in response to the pseudo-grant signal (after asserting signal GNT CHNLA, arbiter 4 returns to its initial state 47 to wait for the next ADD/REQ signal from each of the master), and for generating a ready signal (CHNLA ACTIVE, for example) to a selected one of the requesting master units.

With regard to claim 4, it is clear that the arbiter 4's the master interface includes at least one generator for generating the pseudo-grant signals (GNT CHNLA) from at least one request signal (ADD/REQ) from all the requesting masters.

With regard to claim 5, it is clear that the master interface including at least one circuit for converting a target slave ready signal (CHNLA RDY) from at least one slave (also slave in Kenny) into a data transfer ready signal (CHNLA ACTIVE, for example) for a selected one of the requesting master units.

With regard to claim 6, it is clear that the ready signal (CHNLA RDY) is for data transfer.

With regard to 7, it is clear that data can only be transferred when the bus is available. In other words, the ready signal (CHNLA RDY) indeed indicates bus availability.

With regard to claim 8, it is clear that in Kenny, the arbiter including a controller interface for requesting at least one slave unit to prepare for data transfer in response to the target information (in Kenny, the target information is the address of the slave, ADD, for example) from the selected one of the requesting masters. Note that all modules as shown in Fig. 1, as in any conventional interconnected modules include respective interface for communication among modules. See also col. 5, line 28 to col. 6, line 21).

With regard to claim 9, it is clear that the controller interface is a slave controller interface which interacts with at least one slave controller of the at least one slave unit. Note that all modules as shown in Fig. 1, as in any conventional interconnected

modules) include respective interface for communication among modules. See also col. 5, line 28 to col. 6, line 21).

With regard to claim 10, it is clear that slave memory 6 includes slave controller to control the slave memory.

With regard to claim 13, each driver layer 12 of each master includes registers 21, 22 and 23. Registers 21, 22, and 23 latch read, address and write data, respectively. A master or system clock FCLK (not shown), is received at terminal 24 to synchronize registers 21, 22 and 23 with timing on the bus.

With regard to claims 14-39, see discussion above, since the subject matter presented in claims 14-39 has already been addressed.

With regard to claim 29, note also that it is clear from the discussion above that the steps of generating the request from the master, receiving the request and generating a virtual channel grant signal from the arbiter 4, supplying information from the master, and preparing for data transfer constitute a first stage and completing and transferring constitute a second stage and the first and second stage occur concurrently.

Claims 11 and 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kenny as discussed above, and further in view of the following.

Kenny, as discussed above, discloses the claimed invention including the use of interface controllers for the arbiter and slave module such as the memory module 6. Kenny does not disclose the use of SDRAM (Synchronous Dynamic Random Access

Memory). However, memory such as SRAM is old and well-known in the art as evidence by the definition of SDRAM provided by Wikipedia.com. cited below. SDRAM is an improvement to standard DRAM in that it retrieves data alternately between two sets of memory. This eliminates the delay caused when one bank of addresses is shut down while another is prepared for reading. It's called "Synchronous" DRAM because the memory is synchronized with the clock speed that the computer's CPU bus speed is optimized for. The faster the bus speed, the faster the SDRAM can be. In other words, SDRAM's timing is synchronized to the system clock. By running in sync to an external clock signal, SDRAM can run at the same speed as the CPU/memory bus. It would have been obvious to one of ordinary skill in the art at the time the invention was made to employ SRAM in memory module 6 of Kenny, since the use of SDRAM is old and well-known, as evidence by the definition of SDRAM provided by Wikipedia.com. cited below, for improving latency. Note also that since the interface controller of the arbiter 4 is in direct communication with the memory slave 6 SDRAM controller, it is clear that controller interface is an SDRAM controller interface which interacts with at least one SDRAM controller of the at least one slave unit.

Response to Arguments

Applicants' arguments filed 5/23/2007 have been fully considered but they are not persuasive.

At the outset, Applicants are reminded that claims subject to examination will be given their broadest reasonable interpretation consistent with the specification. *In re*

Morris, 127 F.3d 1048, 1054-55 (Fed. Cir. 1997). In fact, the "examiner has the duty of police claim language by giving it the broadest reasonable interpretation." *Springs Window Fashions LP v. Novo Industries, L.P.,* 65 USPQ2d 1862, 1830, (Fed. Cir. 2003). Applicants are also reminded that claimed subject matter not the specification, is the measure of the invention. Disclosure contained in the specification cannot be read into the claims for the purpose of avoiding the prior art. *In re Sporck*, 55 CCPA 743, 386 F.2d, 155 USPQ 687 (1986).

With this in mind, the discussion will focus on how the terms and relationships thereof in the claims are met by the references. Response to any limitations that are not in the claims or any arguments that are irrelevant and/or do not relate to any specific claim language will not be warranted.

The 112 Rejection:

The rejection under 112, 1st paragraph is hereby withdrawn in view of Applicants' argument.

The 101 Rejection:

The rejection of claims 25 and 33 is hereby withdrawn in view of Applicants' argument.

The Kenny 102 Rejection:

Applicants' amendments overcome the 35 USC 102 Rejection.

Applicants' arguments are moot in view of the new ground of rejection set forth above.

Relevant Art

US Patent Nos. 4,481,572 to Ochsner, 5,935,234 to Arimilli et al., 6,763,415 to Tischler, 7,143,220 to Edirisooriya et al., and 6,691,193 to Wang et al. are cited as relevant art.

Contact Information

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Khanh Dang whose telephone number is 571-272-3626. The examiner can normally be reached on Monday-Friday from 9:AM to 5:PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mark Rinehart, can be reached on 571-272-3632. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should

you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Khanh Dang
Primary Examiner